UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,190,219 B2
APPLICATION NO. : 10/759426
DATED : March 13, 2007
INVENTOR(S) : Burns et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Cover Page

At section (63), under Related U.S. Application Data, "Jul. 30, 2001" should be replaced with --Jul. 3, 2001--.

Drawings

In Figure 1, please replace the up-stream channels reference number "120" with --119--.

Column 2

At line 54, please replace "up-stream channels **118**" with --up-stream channels **119**--.

Column 3

Please delete lines 48-58 and replace with the following paragraph:

-- Looking now to FIG. 3A, automatic gain control logic decoder 204 is illustrated as comprising automatic gain control amplifiers 350 and a logic circuit array 352. Automatic gain control amplifiers 350 accept automatic gain control voltage 114 and output a plurality of comparator outputs 312(n) which are routed to logic circuit array 352. Logic circuit array 352 outputs the plurality of amplifier control signals. As illustrated in FIG. 3B, automatic gain control amplifiers 350 are preferably comprised of a resistor ladder 302 and thirty-five high-gain, low frequency amplifiers 306.1 through 306.35, and logic circuit array 352 is preferably comprised of thirty-five logic circuits 308.1 through 308.35. Resistor ladder 302 is comprised of a top resistor 303, thirty-four resistors designated as resistors 304.1 through 304.34, and a bottom resistor 305. Top resistor 303 is connected on a first side to a bias potential VDD and on a second side to a first side of resistor 304.1. The connection point between top resistor 303 and resistor 304.1 is node 301.1. A second side of resistor 304.1 is connected to a first side of resistor 304.2 at a node 301.2. Thus it can be said that for any sequential pair of resistors 304(i) and 304(i+l) in resistor ladder 302, a second side of resistor 304(i) is connected to a first side of resistor 304(i+l) at node 301 (i+l). At the "bottom" of resistor ladder 302, a second side of resistor 304.34 is preferably connected to a first side of bottom resistor 305 at node 301.35, and a second side of bottom resistor 305 is preferably connected to a ground 309. Those skilled in the relevant art(s) will understand, based on the teachings contained herein, that the second side of bottom resistor 305 could be connected to a potential other than ground without deviating from the spirit and intent of the invention. Further, the invention also covers the embodiment wherein the first side of resistor 304.1 is connected directly to bias potential VDD 307, and the second side of resistor 304.34 is connected directly to ground 309. --

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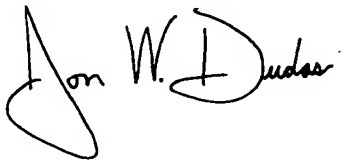
Column 15
At line 41, please insert a period after "settings)".
At line 50, please insert a period after "off".

Signed and Sealed this

Sixteenth Day of September, 2008



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Director of the United States Patent and Trademark Office